# Lab 4

# Memory

In this lab we will once again replicate what was done in class. The goal is to create a basic 4x4 Bit memory. You will be using parts of this lab to complete Assignment 2.

Part 1.

Lets build a basic SR latch (top right) and package it up. The bottom, circuit is the SR latch is used as part of a D-latch with an enable. Create these, circuits, finishing with the enabled D-latch package below.





Part 2

With a basic 1 bit memory, we can create larger circuits. Here we will create a 1x4 (1 word x 4 bits) chip. The principle of operation: Qout will always output what is stored in the latches. Only when new input is allowed to overwrite the latches will Qout change. The **En**able line can be viewed as a write / control line. Not exactly industry standard but it will have to do.



Part 3

To go further we need to build a new component. We require a 2 to 4 decoder with an Enable line. Recall that you created a 2 to 4 decoder in Lab 2 part 1 with the address lines combined. Copy that circuit into a new circuit called 2 to 4 decoder with enable. Modify it so AND gates control the output of the decoder. This part can be tricky. The TA will guide you through the process.

Part 4

We are now ready to create a 4x4 memory. To the right is a simple 4x4 memory. It is built from the components we have created so far. Once you create the package, test the package with the below circuit. Note the bit widths of the inputs, and outputs. Probes and sensors require matching bit widths.



Part 5.

The issue with the above memory is that it has 4 distinct 4 bit outputs. Let us combine these outputs to a single output. For this to happen we need to introduce a new component, the tri-state buffer device. Unlike other devices which would be 2 state devices, either a 0 or 1, a tristate has 3 possible outputs, 0, 1 or not connected. When the control pin on the bottom is high, the output will reflect the input. When the control pin is low, the output goes into a state of not connected. Create a package which resembles the lower right circuit. Once completed you can create the below circuit, and then test it, bottom right.



