

Cell Processors and the Sony PlayStation 3

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Introduction

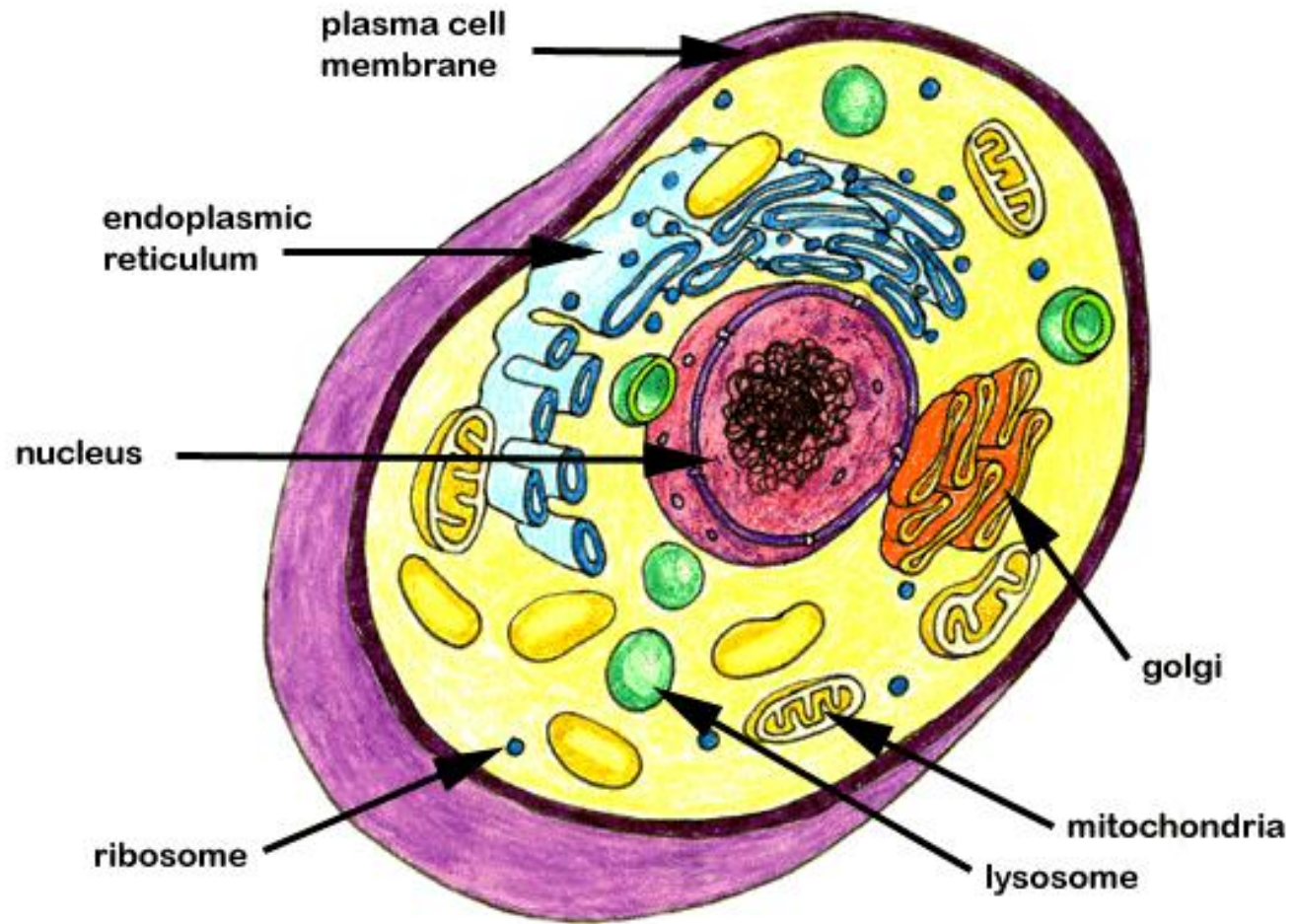
Background Info & What is a Cell?

- Started in 1999 with an idea from Sony's Ken Kutaragi (Father of the PlayStation).
- Sony officially partnered with Toshiba and IBM in 2000 to build the cell processor.
- Development of the Cell Processor was done in 10 centres around the globe by some 400 people from Sony, Toshiba and IBM over a 4 year period.
- Uses for Cell Processors:
 - ✓ Game Consoles (PS3)
 - ✓ Blu-ray Players
 - ✓ HDTVs, HD Camcorders
 - ✓ High End Servers (IBM BladeCenter QS21)

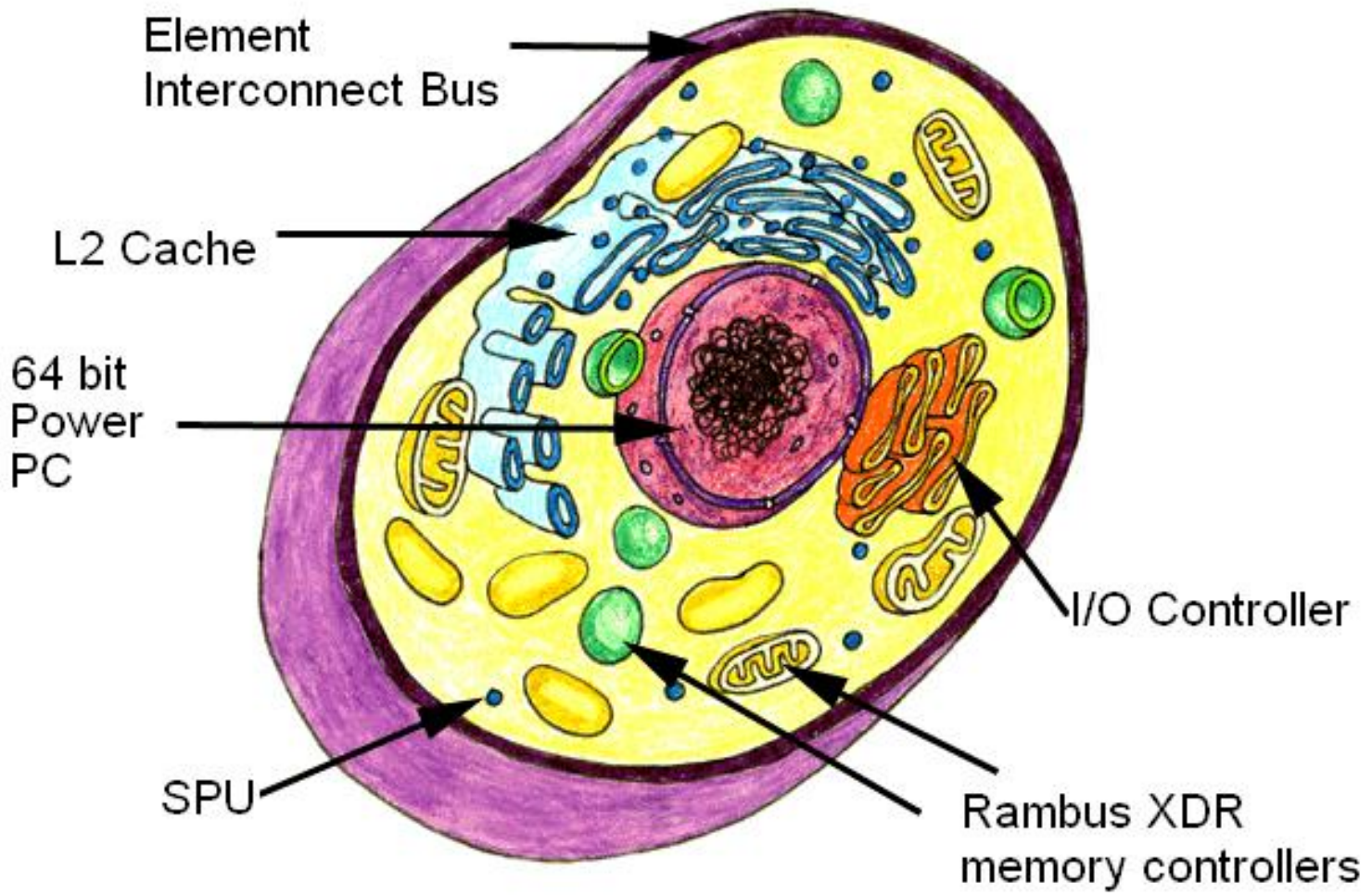
- The estimated development cost was about \$400 Million USD.

- A **cell processor** (also known as **Cell Broadband Engine Architecture (CBEA)**) is a heterogeneous single chip consisting of:
 - “IBM 64-bit Power Architecture™ core, augmented with eight specialized co-processors based on a novel single-instruction multiple-data (SIMD) architecture called Synergistic Processor Unit (SPU)”
 - The system is integrated with a high-speed on-chip bus.

What is a Cell 2?



What is a Cell 3?



How It Works

PPE, SPE, Bus & Controllers

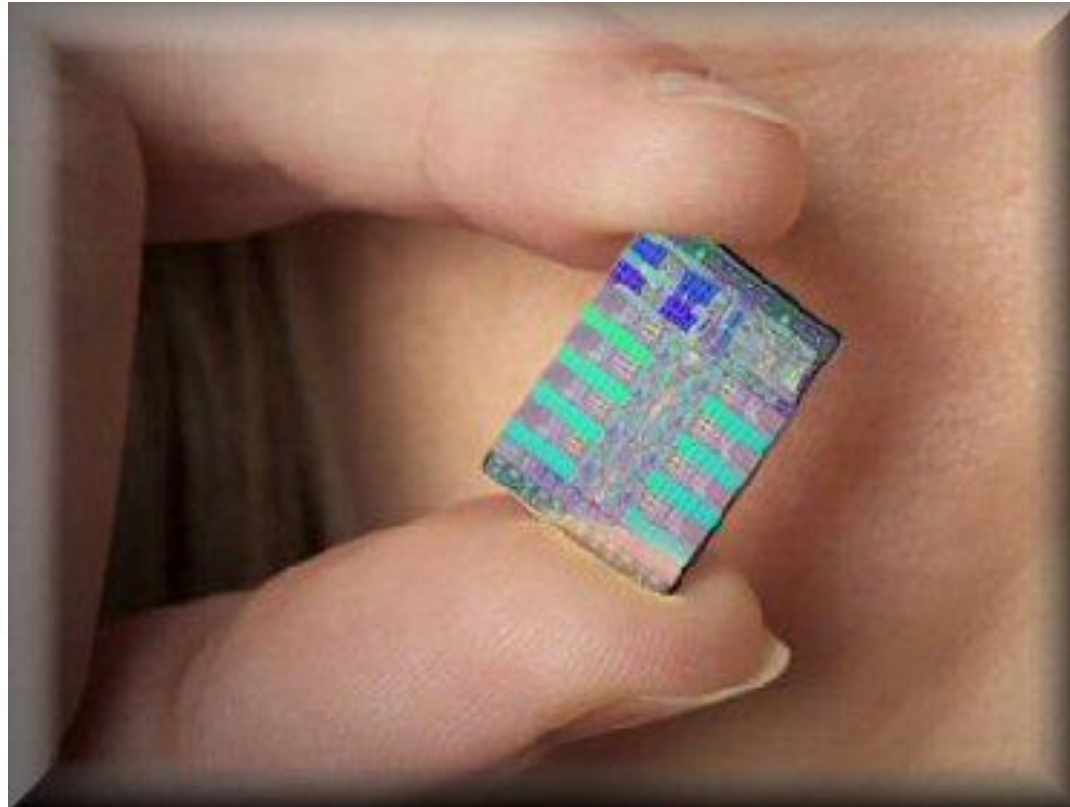
A cell processor typically contains the following components:

1. Power Processing Element (PPE)
2. Synergistic Processing Element (SPE)
3. Element Interconnect Bus (EIB)
4. Memory Interface Controller (MIC)
5. Broadband Engine Interface (BEI)

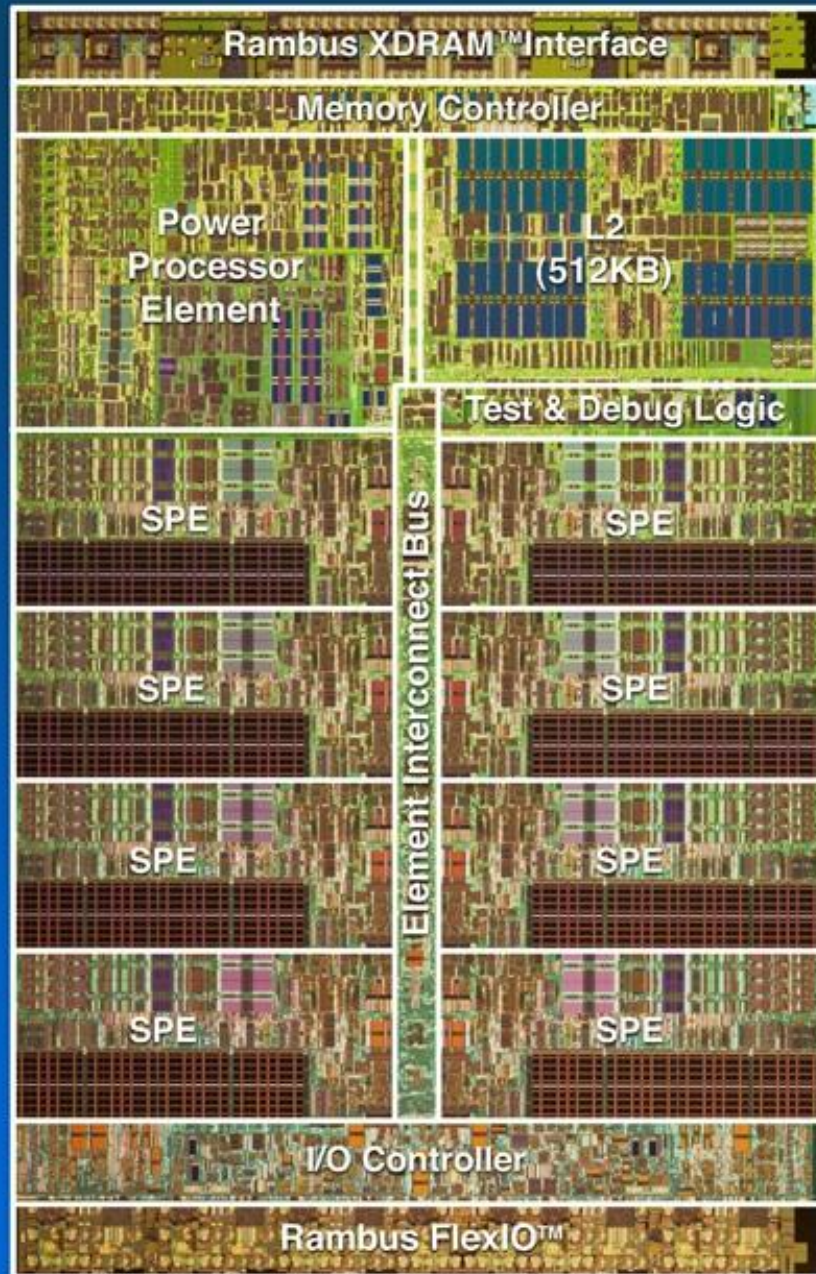
Transistor Count: **234 million**

Die Area: **221mm²**

Size of the Cell



Cell Broadband Engine Processor



PPE – Power Processing Element

- PowerPC based, running @3.2GHz
- 64-bit
- 64 KB of L1, and 512KB L2
- dual threaded, in-order processor
- Supports Hypervisor Technology
- Supports VMX® SIMD instruction set
- Slower than G5

SPE - Synergistic Processing Element

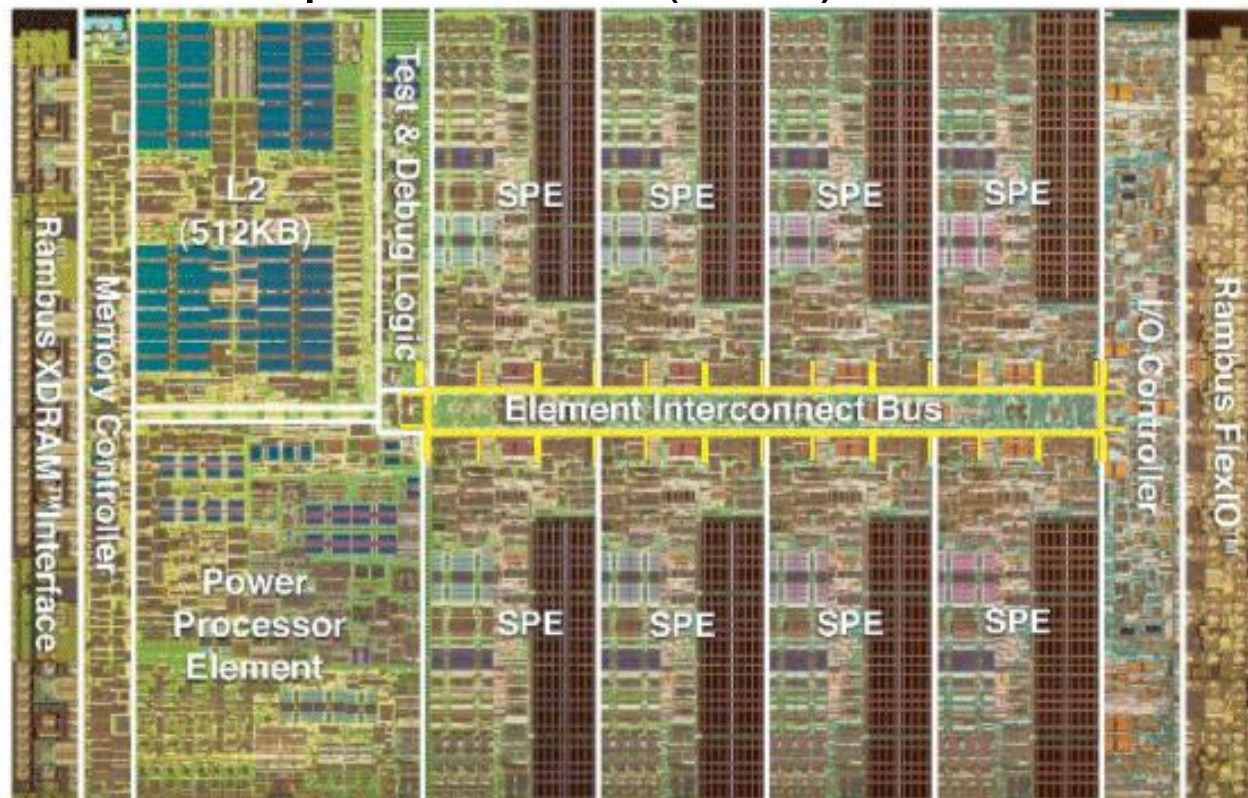
- SIMD processor capable of vector and scalar operation, runs @3.2GHz
- Big Endian
- 128 Registers of 128 bits
- 256KB Local storage (SRAM)
- 21 million transistors: 14M SRAM and 7M logic
- 32 bit wide instruction
- ISA is similar to VMX, but is not a derivative
- Does **not** comply with IEEE 754 for single-precision operation (eg. No INF)

- For double-precision, only a subset of the operations required by the IEEE standard is supported in hardware.
- No support for virtual memory
- No direct main memory access; SPE can only load data from main memory to local store through Memory Flow Controller.
- Has extremely limited interrupt support
- Each SPE has its own Local Store which cannot be directly accessed by other SPEs.

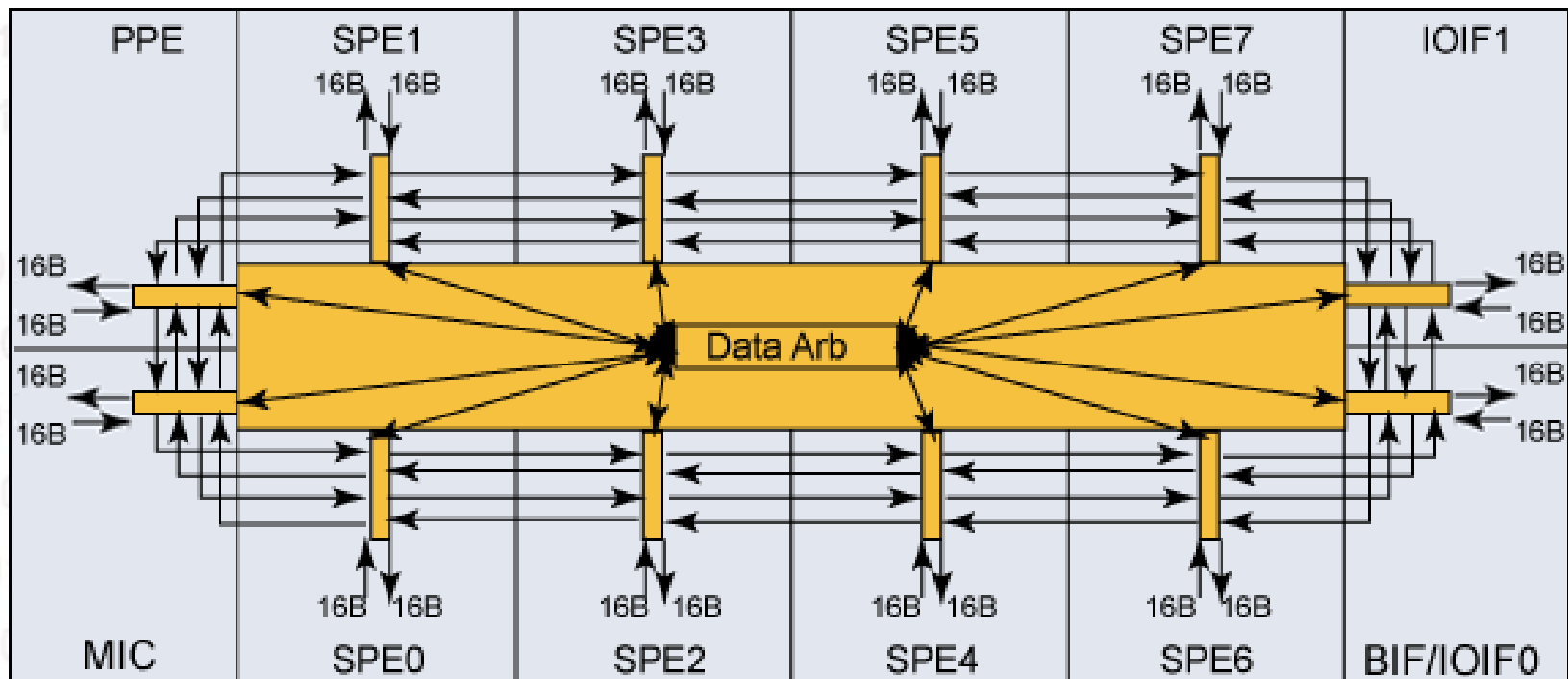
- Local store's address is 32-bit
- Aligned on 16-byte boundary; can only load 16 bytes at a time
- In PS3, one of the 8 cores is disabled, and one is reserved for system usage (resulting in 6 left over for computation)

Element Interconnect Bus

- Provides for the huge bandwidth demands of the components (PPE, SPEs, Controllers)
- 25.6GB/s per element (MAX)



- Implemented as a circular ring comprised of four 16 Byte wide unidirectional channels (2 clockwise, 2 counter-clockwise).
- EIB runs at half the system clock rate.



Bottlenecks

- The 4 rings are a shared resource.
- Odd numbered SPEs accessing the MIC means degraded bus services for the PPE.
- The further apart two components are on the rings, the more expensive communication between them will be.
- One key feature is that the PPE and MIC are adjacent, so communications between them can generally occur with minimal disruption of other communications.

MIC – Memory interface controller

- Interface between EIB and physical memory
- Supports two channels of XDR memory for a total of 64 MB to 64 GB of RAM
- Max memory bandwidth is 25.6GB/s
- The memory interface runs at 3.2 Gigabits/second per pin

BEI – Cell Broadband Engine Interface

- Manages data transfers between Processor Elements on EIB and I/O devices
- Supports two Rambus FlexIO I/O interfaces
- One interface only supports non-coherent I/O Interface (IOIF) protocol, which is suitable for standard I/O devices
- The other interface supports both non-coherent IOIF protocol *and* fully coherent Cell BIF protocol

- BIF is the EIB's native internal protocol, which can be used to connect two CBEA Processor
- BIF - Cell Broadband Engine interface protocol
- CBEA - Cell Broadband Engine™ Architecture

Other Uses for the Cell

- **Healthcare / Life Sciences**

- X-ray, MRI, Endoscope, Ultrasound
- Reduced execution time from 48 sec on 3Ghz P4 to 0.28 sec on Cell.

- **Financial Modelling**

- Risk Assessment, Portfolio Analysis, Algorithmic Trading
- Increase executing by factor of 12x

- **Digital Media**

- IPTV, Blu-Ray Authoring
- Security Camera
- Rendering
- Ray Tracing

- **Manufacturing Processes**

- Semiconductor Package Inspection
- Liquid Crystal Panel Inspection
- Glass Substrate Inspection
- Printed Circuit Board Inspection

- [http://www-01.ibm.com/chips/techlib/techlib.nsf/techdocs/1AEEE1270EA2776387257060006E61BA/\\$file/CBEA_v1.02_11Oct2007_pub.pdf](http://www-01.ibm.com/chips/techlib/techlib.nsf/techdocs/1AEEE1270EA2776387257060006E61BA/$file/CBEA_v1.02_11Oct2007_pub.pdf)
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